REMARKS

Claims 1-34, all the claims pending in the application, stand rejected on prior art

grounds. Applicants respectfully traverse these rejections based on the following

discussion.

I.   The Prior Art Rejections

Claims 1-34 stand rejected under 35 U.S.C. §102(b) as being anticipated by

Blaner, et al., "AN EMBEDDED PowerPC SOC for Test and Measurement

Applications," 13th Annual IEEE International ASIC/SOC Conference, 2000, September

13-16, 2000, pages 204-208, hereinafter referred to as Blaner. Claims 1-34 stand rejected

under 35 U.S.C. §102(e) as being anticipated by Devins, et al. (U.S. Patent No.

NUMBER), hereinafter referred to as Devins. Applicants respectfully traverse these

rejections based on the following discussion.

The claimed invention a method and structure for a verification testbench system

for testing an interface of a system-on-a-chip (SOC), comprising a verification interface

model connected to the SOC interface. In the rejection, the Office Action argues that

Blaner discloses a memory-mapped external device containing software readable and

writable registers that appear as wires in a testbench, which is connected to an external

bus. In addition, the Office Action argues that Devins discloses external bus interface

logic coupled to a SOC device via a chip-external bus. However, neither Blaner nor

Devins disclose *connecting the testbench to an external SOC via the SOC interface and

the model interface (independent claims 1, 8, 15, 21, and 28)*. Moreover, neither Blaner

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nor Devins disclose *a test case in the SOC that can use the same software driver to program both the SOC interface and the model interface (dependent claims 4, 11, 17, 24, and 31)*. Therefore, as explained in greater detail below, Applicant respectfully submits that the prior art of record does not teach or suggest the claimed invention.

A.   Blaner

The Office Action argues that Blaner's has the ability to connect a memory-mapped external device, which contains software readable and writable registers that appear as wires in a testbench, to an external bus (p. 208, column 1, para. 2). However, nothing in Blaner mentions connecting the testbench to an external SOC via the model interface and the SOC interface. The "memory-mapped external device" of Blaner is not synonymous with the "model interface" of Applicant's invention. Specifically, in Blaner, the "memory-mapped external device" is used to synchronize external activity to internal software.

To the contrary, as described in paragraph 23 of Applicant's disclosure, the invention transfers data from the external interface model 210 to the SOC interface 101. The test case calls the software driver (SWD) 135-137 for the interface 101 and instructs the software driver to configure the interface 101 to receive data. Next, the test case calls the same SWD 135-137 and instructs the software driver to configure the external interface model 210 to send data. The SOC's interface 101 and the external interface model 210 are implemented to respond to different unique addresses. Thus, when the test case calls the SWD 135-137 to perform some configuration on one of the interfaces, the

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test case sends the address of that interface along with the operation to be performed. The

test case then sends test data to the unique data address of the external interface model

210. This data is sent from the SOC 100 through the SOC's external bus interface unit

(EBIU) 205 to the external EBIU 200 and then along to the interface model 210. From

there the data is sent through the interface model 210 into the SOC's interface 101 which

is configured to receive data. Once the data is back in the SOC 100, the test case checks it

for correctness and a test status is recorded.

In addition, the Office Action argues that Blaner's has the ability to use an EBIU

to control up to eight banks of mixed types of memories and to operate at one-half the

PLB clock frequency (p. 205, column 2, para. 3). Further, Blaner explains that the EBIU

allows an off-chip device, called the external bus master, to take ownership of the

external bus and access attached memories (p. 205, column 2, para. 3). However, nothing

in Blaner mentions a test case in the SOC that can use the same software driver to

program both the SOC interface and the model interface. As described in paragraph 24

of Applicant's disclosure, the invention allows **the test case executing in the SOC 100**

to use the same software driver, if appropriate, to program both interfaces 101, 210

(to configure and control the SOC interface and the verification interface model). The

test case can also use one driver to program the SOC interface 101 and another to

program the interface model 210, both of which are controlled by the test case

(a test case running in the SOC to control both the SOC interface and the verification

interface model). This is an improvement over the conventional situation where the test

case running within the SOC 100 controls the SOC interface 101, and another software

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program (written in a bus functional language) controls the external interface 210. The invention provides increased reusability and decreased development time because the invention uses the same or similar software written in the same language to program both interfaces (the same software driver to configure and control the SOC interface and the verification interface model).

Furthermore, as described in paragraph 26 of Applicant's disclosure, the invention represents a clean way of controlling external interfaces without the need for a complex control mechanism such as the conventional semaphore derived scheme used to enable communication between the SOC being tested and the external interface. The external bus mastering of the test bench EBIU 200 allows external model programming from the SOC test case. **Thus, the same test case directly controls operations of the SOC interface 101 and the external model 210** (a test case running in the SOC to control both the SOC interface and the verification interface model).

Nothing in Blaner teaches the foregoing features of Applicant's invention, namely a test case in the SOC that can use the same software driver to program both the SOC interface and the model interface. The fact that Blaner discloses, on page 205, column 2, paragraph 3, an external bus master for taking ownership of the external bus and accessing attached memories has nothing to do with programming both the SOC interface and the model interface with the same software driver.

The Office Action also relies on the EBIU in Blaner to reject Applicant's claims directed towards an SOC EBIU that allows a test case running in the SOC to control both the SOC interface and the verification interface model (i.e., dependent claims 2, 9, 16, 22,

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and 29); and, the SOC interface and the verification interface model, which are both programmed by a test case running in the SOC (i.e., independent claim 15 and dependent claims 3, 10, 23, and 30). Specifically, the Office Action relies on argues that Blaner's has the to use the EBIU to: (1) control up to eight banks of mixed types of memories; (2) operate at one-half the PLB clock frequency; and, (3) allow the external bus master to take ownership of the external bus and access attached memories (p. 205, column 2, para. 3). Again, the Office Action argues that Blaner discloses, on page 205, column 2, paragraph 3, an external bus master for taking ownership of the external bus and accessing attached memories, which has nothing to do with an SOC EBIU that allows a test case running in the SOC to control both the SOC interface and the verification interface model; and, the SOC interface and the verification interface model, which are both programmed by a test case running in the SOC.

Blaner broadly discloses a design for an SOC and briefly discusses how it was tested. Blaner includes many details of how code was structured for re-useablility across the many SOC designs and how simulation is accelerated by modeling the processor in the RTX code, rather than using the HDL model of the processor. However, Blaner specifically does not disclose building a testbench to stimulate/monitor the chip's I/O.

Therefore, contrary to the position taken in the Office Action, Applicant submits that Blaner does not teach or suggest connecting the testbench to an external SOC via the SOC interface and the model interface; and, a test case in the SOC that can use the same software driver to program both the SOC interface and the model interface. Further, Blaner does not teach or suggest an SOC EBIU that allows a test case running in the SOC

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to control both the SOC interface and the verification interface model; and, the SOC interface and the verification interface model, which are both programmed by a test case running in the SOC.

Thus, it is Applicant's position that Blaner does not disclose or suggest the claimed feature of "a verification interface model connected to said SOC interface" as defined by independent claims 1, 8, 15, 21, and 28; and the claimed feature of "said test case utilizes the same software driver to configure and control said SOC interface and said verification interface model" as defined by dependent claims 4, 11, 17, 24, and 31. Further, Blaner does not disclose or suggest the claimed feature of "said SOC EBIU allows a test case running in said SOC to control both said SOC interface and said verification interface model" as defined by dependent claims 2, 9, 16, 22, and 29; and the claimed feature of "said SOC interface and said verification interface model are programmed by a test case running in said SOC" as defined by independent claim 15 and dependent claims 3, 10, 23, and 30. Moreover, Applicant submits that because Applicant's broadest claim, i.e., independent claim 1, is patentable over the prior art, the remaining narrowing claims are therefore patentably distinct over the prior art.

B.   Devins

With respect to Devins, the Office Action proposes that Devins' has the ability to couple external bus interface logic of a device to the SOC device via a chip-external bus. However, nothing in Devins mentions connecting the testbench to an external SOC via the model interface and the SOC interface. The "external bus interface logic" of Devins is not synonymous with the "model interface" of Applicant's invention; rather, as pointed

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out on page 12, item 27 of the Office Action, "[t]his corresponds to the 'test bench external bus interface unit (EBIU)'".

The Office Action also relies upon Devins' external bus interface logic 202 to reject Applicants claims towards (1) a test case that utilizes the same software driver to configure and control the SOC interface and the verification interface model (i.e., dependent claims 4, 11, 17, 24, and 31); (2) an SOC EBIU that allows a test case running in the SOC to control both the SOC interface and the verification interface model (i.e., dependent claims 2, 9, 16, 22, and 29); and (3) the SOC interface and the verification interface model, which are programmed by the test case running in the SOC (i.e., independent claim 15 and dependent claims 3, 10, 23, and 30). Specifically, the Office Action highlights Devins' external bus interface logic 202, which is designed to direct signals received via connection 107 to the appropriate logical address, and to convert the particular bus protocol received into an internally-used format applicable to the command decode logic 203 (column 4, lines 15-20 and 38-40; column 5, lines 5-8).

Once more, the features cited in the prior art reference have nothing to do with utilizing the same software driver to configure and control the SOC interface and the verification interface model. Further, Devins does not mention allowing a test case running in the SOC to control both the SOC interface and the verification interface model; nor does Devins mention programming both the SOC interface and the verification interface model by the test case running in the SOC.

Thus, it is Applicant's position that Devins does not disclose or suggest the claimed feature of "a verification interface model connected to said SOC interface" as

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defined by independent claims 1, 8, 15, 21, and 28; and the claimed feature of "said test case utilizes the same software driver to configure and control said SOC interface and said verification interface model" as defined by dependent claims 4, 11, 17, 24, and 31. Further, Devins does not disclose or suggest the claimed feature of "said SOC EBIU allows a test case running in said SOC to control both said SOC interface and said verification interface model" as defined by dependent claims 2, 9, 16, 22, and 29; and the claimed feature of "said SOC interface and said verification interface model are programmed by a test case running in said SOC" as defined by independent claim 15 and dependent claims 3, 10, 23, and 30. Moreover, Applicant submits that because Applicant's broadest claim, i.e., independent claim 1, is patentable over the prior art, the remaining narrowing claims are therefore patentably distinct over the prior art.

Therefore, it is Applicant's position that neither Blaner nor Devins teach or suggest many features defined by independent claims 1, 8, 15, 21, and 28 and that such claims are patentable over the prior art of record. Further, it is Applicant's position that dependent claims 2-7, 9-14, 16-20, 22-27, and 29-34 are similarly patentable, not only because of their dependency from patentable independent claims, but also because of the additional features of the invention they defined. In view of the foregoing, the Examiner is respectfully requested to reconsider and withdraw this rejection.

II.   Conclusion

In view of the foregoing, the Examiner is respectfully requested to reconsider and withdraw the rejections to the claims. Accordingly, Applicants submit that claims 1-34

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are patentably distinct from the prior art of record and are in condition for allowance. The Examiner is respectfully requested to pass the above application to issue at the earliest possible time. Should the Examiner find the application to be other than in condition for allowance, the Examiner is requested to contact the undersigned at the local telephone number listed below to discuss any other changes deemed necessary. Please charge any deficiencies and credit any overpayments to Attorney's Deposit Account Number 09-0456.

Respectfully submitted,

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Duane N. Moore
Registration No. 53,352

Gibb Intellectual Property Law Firm, LLC
2568-A Riva Road, Suite 304
Annapolis, MD 21401
Voice: (410) 573-6501
Fax: (301) 261-8825
Customer Number: 29154

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